

Eylon Caspi

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- OBJECTIVE** Full time position in design automation, compilers, and/or architecture for novel digital systems
- EDUCATION**
- Ph.D. (in progress) Computer Science, University of California, Berkeley
Berkeley Reconfigurable Architectures, Systems and Software (BRASS) group
Thesis topic: Design automation for streaming systems
Minors: Digital signal processing, quantum mechanics
 - M.S. (Dec. 2000) Computer Science, University of California, Berkeley
Project: Empirical study of opportunities for bit-level specialization in C
 - B.S. (May 1996) Electrical Engineering (summa cum laude)
 - B.S. (May 1996) Computer Science (magna cum laude)
University of Maryland, College Park
Concentration: Digital signal processing, VLSI design, computer architecture
- WORK EXPERIENCE**
- Software engineer, half time, Chameleon Systems (San Jose, CA, Nov. 2000–Jan. 2003)
- Designed algorithms to compile data flow graphs for the Chameleon reconfigurable processor
 - Wrote internal technical reports and patent application on compilation methodology
- Teaching assistant, U.C. Berkeley (Berkeley, CA, Jan.–May 2000)
- Head teaching assistant for a digital design course with a project to implement a MIDI sound synthesizer on an FPGA board
 - Devised and revised laboratory assignments, supervised laboratory work, lectured, graded exams, maintained course home page
- Summer intern, Intel Corp. (Santa Clara, CA, May–Aug. 1997)
- Designed, implemented, and documented Perl programs to integrate and support design flow for a state-of-the-art VLSI CMOS cell library
- Summer intern, Naval Research Laboratory, Information Technology Division (Washington D.C., May–Aug. 1996)
- Designed and implemented a graphical user interface (using TAE+ for X/Motif) for *SCR-Tool*, a software tool for formal specification and verification of control systems
- Co-op, IBM, Personal Systems Division (Boca Raton, FL, Jan.–July 1994)
- Tested and documented installation software for OS/2 for PowerPC
 - Set-up and maintained a server to automatically compile department code nightly
- ADDITIONAL SKILLS**
- Programming Languages: C, C++, Java, Perl, csh, SML, Lisp, Pascal, BASIC, Prolog
- Hardware design environments: Verilog, ModelSim, Synplify Pro, Xilinx ISE, Magic, SPICE
- Compiler design environments: SUIF, lex, yacc, tdfc (custom compiler for my Ph.D.)
- Course projects related to digital design, CAD, compilation:
- Designs for FPGA: MIDI sound synthesizer, floating point adder, IDEA encryption
 - Compiler analysis of bounded memory usage in process networks
 - Task scheduling for a reconfigurable device with paged, virtual hardware
 - Routing for a fat-tree FPGA interconnect
 - 1D placement/routing optimizer for Garp
 - Compiler analysis of bit usage in C variables
 - 7-bit microprocessor in *SFL* HDL, fabricated in 2μ CMOS
 - Custom CMOS layout: systolic array for matrix multiplication, pipelined floating point adder
 - Obstacle avoiding behavior for an autonomous, floor-vacuuming robot
- HONORS**
- GAANN graduate fellowship (U.C. Berkeley, Sept. 1996)
- Undergraduate Research Participation Award, Institute for Systems Research (U. MD, Jan. 1995)
- Member Eta-Kappa-Nu, Tau-Beta-Pi, Phi-Kappa-Phi national honors societies